RapidChip Technology Propels Trimble's GPSEngine to State-Of-The-Art

Fast time to market,75% NRE and 50% engineering time-savings are major benefits

"Our design schedule was of utmost concern, and that was one reason we chose the RapidChip Platform ASIC so we could achieve quick time to market."

Ron Smith
General Manager. Military and Advanced Systems, Trimble

The Opportunity

Trimble's Military and Advanced Systems (MAS) likes to exploit new opportunities. Plus, they're intent on maintaining a highly competitive market posture in military global positioning systems (GPS) and providing its system integrator customers with leading edge products and technology.

A case in point is its new Force 524 GPS receiver designed for embedded applications such as inertial navigation systems. The Force 524 receiver has 24 channels, 24 correlators per channel, and a massive parallel acquisition correlator array to dramatically accelerate the process of acquiring and locking on satellite signals. The GPS has provisions to work with digital antennas so that it can continue to provide positioning data even in a jamming environment.

Related Information

Products

- RapidChip Platform ASIC

Markets

- Communications

More Information

- Printable PDF Version

Ron Smith, general manager for Trimble's MAS, said, "The heart of this GPS receiver is a RapidChip technology-based 24 channel GPS engine that's state-of-the-art, plus it introduces capabilities that other GPS products don't presently offer."

He added, "Our design schedule was of utmost concern, and that was one reason we chose the RapidChip Platform ASIC so we could achieve quick time to market. Also, RapidChip technology provided us a 75 percent NRE savings compared to cell-based ASIC development, plus a 50 percent savings in engineering development time. And thanks to the highly integrated RapidChip Platform ASIC, we went from an 11 die multi-chip module to a six die module."

Turbo-Charging TheTracking Channels

The GPS engine design solution for the new GPS receiver is from the RapidChip™ Integrator™ Platform ASIC family. In this instance, the single chip RC11Si231 replaces six chips supporting similar functionality in an earlier model. The RC11Si231 RapidChip Platform ASIC sports 3.5 million usable gates, 2.5 megabits of memory, and an ARM926 processor with 100 MIPS capability to turbo-charge six major on-chip GPS engine functions Trimble MAS engineers designed into the RapidChip logic.

One of the key advantages of the RC11Si231 RapidChip Platform ASIC is the Landing Zone™. This is an area of the chip that is ready to accept an ARM or MIPS processor with different memory configurations for different sizes and arrangements of cache, allowing designers to tailor the chip to their system requirements.

Included are a compute-intensive direct P (Y) code signal acquisition accelerator and 24 tracking channels supported by a massively parallel acquisition correlator array. These advanced functions are the linchpin for highly accurate GPS measurement.

"Our new 24 channel GPS engine has the ability to simultaneously track L1 and L2 frequencies each GPS satellite transmits simultaneously. But more importantly, it provides a higher degree of integrity for the signals," Smith stated.

A key element in direct P (Y) code acquisition is the number of correlator channels and processing elements in a GPS receiver to match locally generated pseudo-random noise (PRN) codes with codes transmitted by satellites. The RapidChip Platform ASIC's ultra high gate count, ample memory, and powerful ARM processor provide the foundation for this GPS engine's massive parallel data processing and bit correlation to substantially increase system performance.

Tom Holden, technical director at Trimble's MAS, said, "This is the biggest channel tracking array that anyone has put together on one chip. While other GPS companies may have designs with 36 or 48 channels, they have far fewer correlators per channel compared to our design and typically use one half to one million gate cell-based ASIC."

Trimble MAS engineers deployed 1.8 million gates of the RC11Si231 chip to implement a DSP-like channel core or correlator array for acquiring and tracking GPS signals. Using another 400,000 gates plus the available diffused memory, they designed the direct P (Y) code acquisition accelerator block that performs searches on over 175,000 code combinations per second.

"The RapidChip Platform ASIC's diffused memory saved us considerable design time when we implemented the direct P (Y) code acquisition function," Holden noted. "In this case, the diffused memory saved us a lot of gates. In the earlier cell-based ASIC design, we used almost a million gates to build this same function because we had to build the memory. But now, since we didn't have to build the memories, we used only 400,000 gates and some of the diffused memory. That diffused memory was a big plus for us."

Setting A New Standard

Smith said, "Force 524 powered by the RapidChip Platform ASIC sets an industry standard for GPS military capability. We've already set the standard for military positioning accuracy and this advancement with the Rapidchip Platform ASIC helps to establish us in an even greater technology leadership role in high-end applications."

At the outset of the GPS engine design, the Trimble MAS strategy was to take a different approach than the high NRE cost cell-based ASIC. It wanted rapid time to market and a lower NRE. Smith noted, "We are very excited about our Force 524 and in particular, the technology advances we've made with our RapidChip technology-based GPS engine. If we play our state-of-the-art product correctly, it'll put us in a top spot relative to other market players."

TOP

E-mail this page | Printer Friendly Format

Home | Product Solutions | Market Solutions | Technology | Support
Downloads | Documentation | Buy online | Partner Resources
Contacts | About LSI | Worldwide